Fig. 1

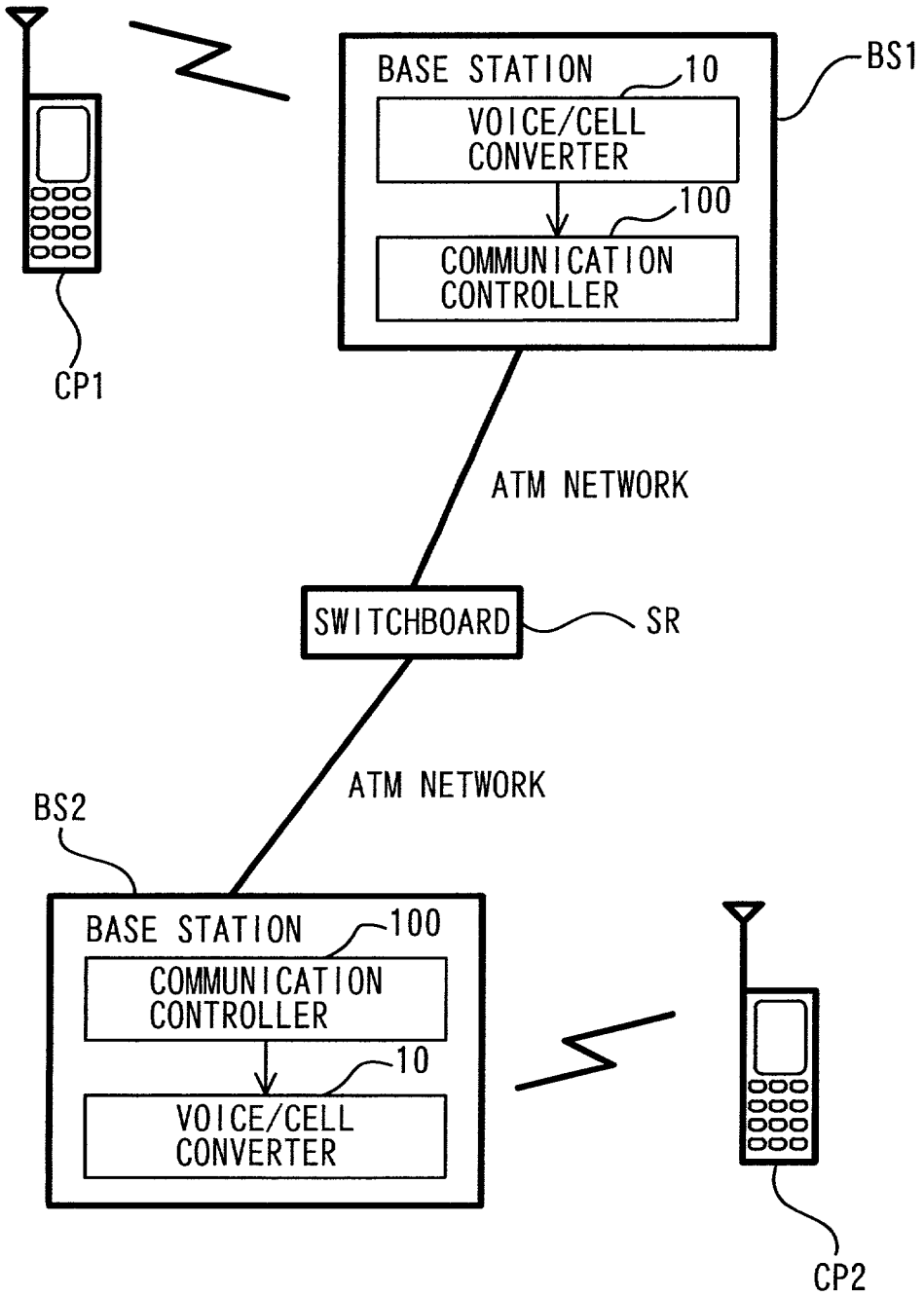

BASE STATION
10
VOICE/CELL CONVERTER
100
COMMUNICATION CONTROLLER
BS1
CP1
ATM NETWORK
SWITCHBOARD
SR
ATM NETWORK
BS2
BASE STATION
100
COMMUNICATION CONTROLLER
10
VOICE/CELL CONVERTER
CP2

Fig. 2

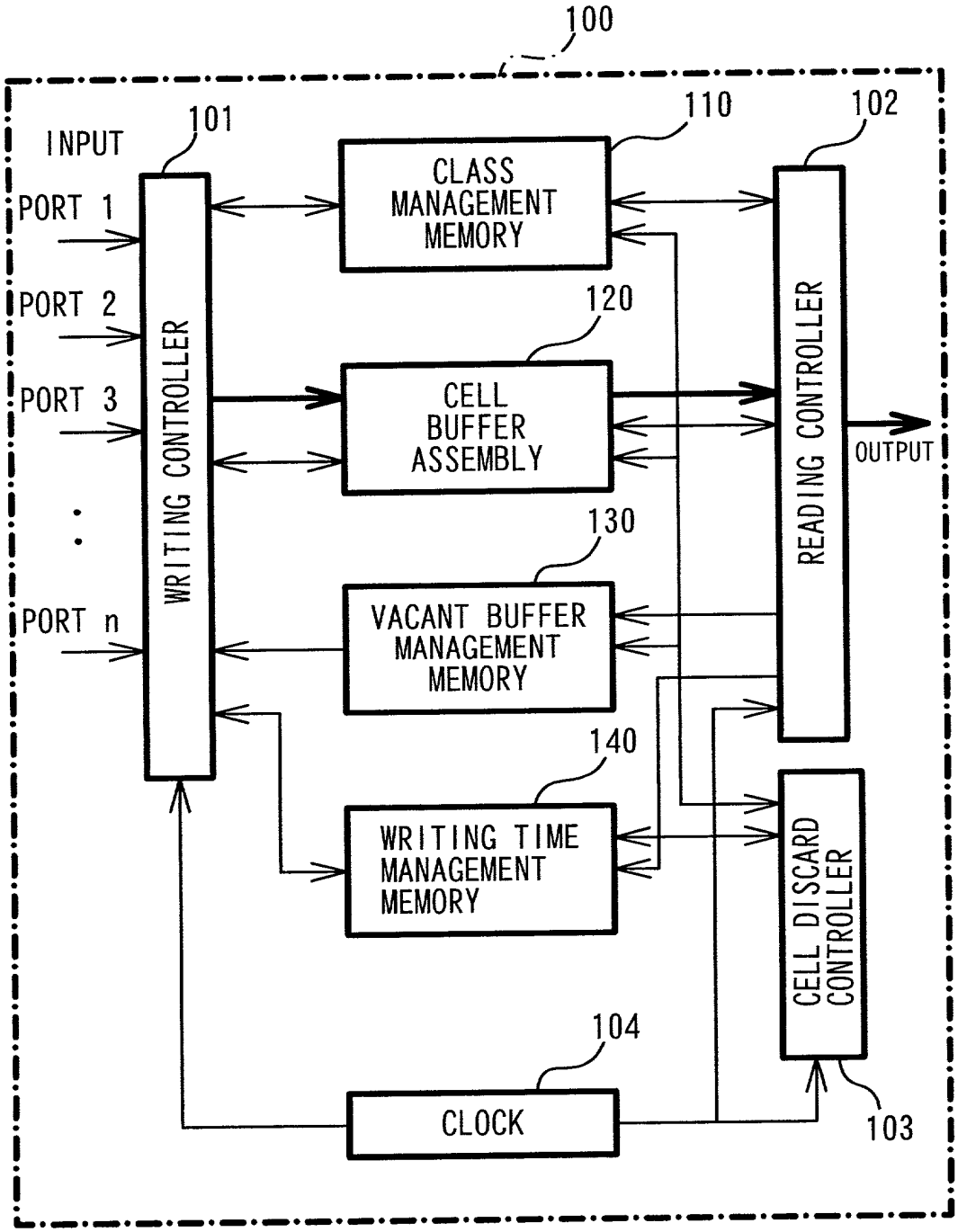

100
INPUT
PORT 1
PORT 2
PORT 3
PORT n
101
WRITING CONTROLLER
110
CLASS MANAGEMENT MEMORY
120
CELL BUFFER ASSEMBLY
130
VACANT BUFFER MANAGEMENT MEMORY
140
WRITING TIME MANAGEMENT MEMORY
102
READING CONTROLLER
OUTPUT
CELL DISCARD CONTROLLER
103
104
CLOCK

Fig. 3

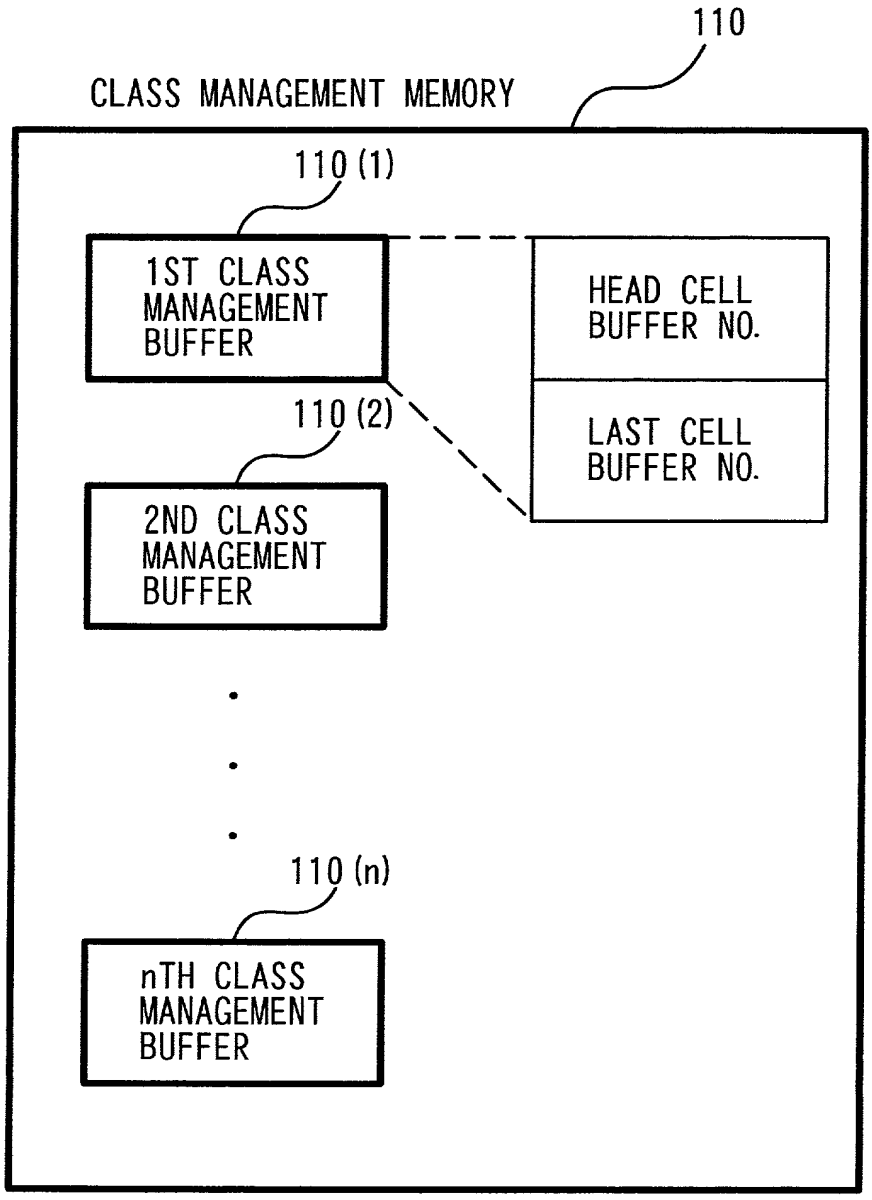

110
CLASS MANAGEMENT MEMORY
110 (1)
1ST CLASS MANAGEMENT BUFFER
HEAD CELL BUFFER NO.
LAST CELL BUFFER NO.
110 (2)
2ND CLASS MANAGEMENT BUFFER
110 (n)
nTH CLASS MANAGEMENT BUFFER

Fig. 4

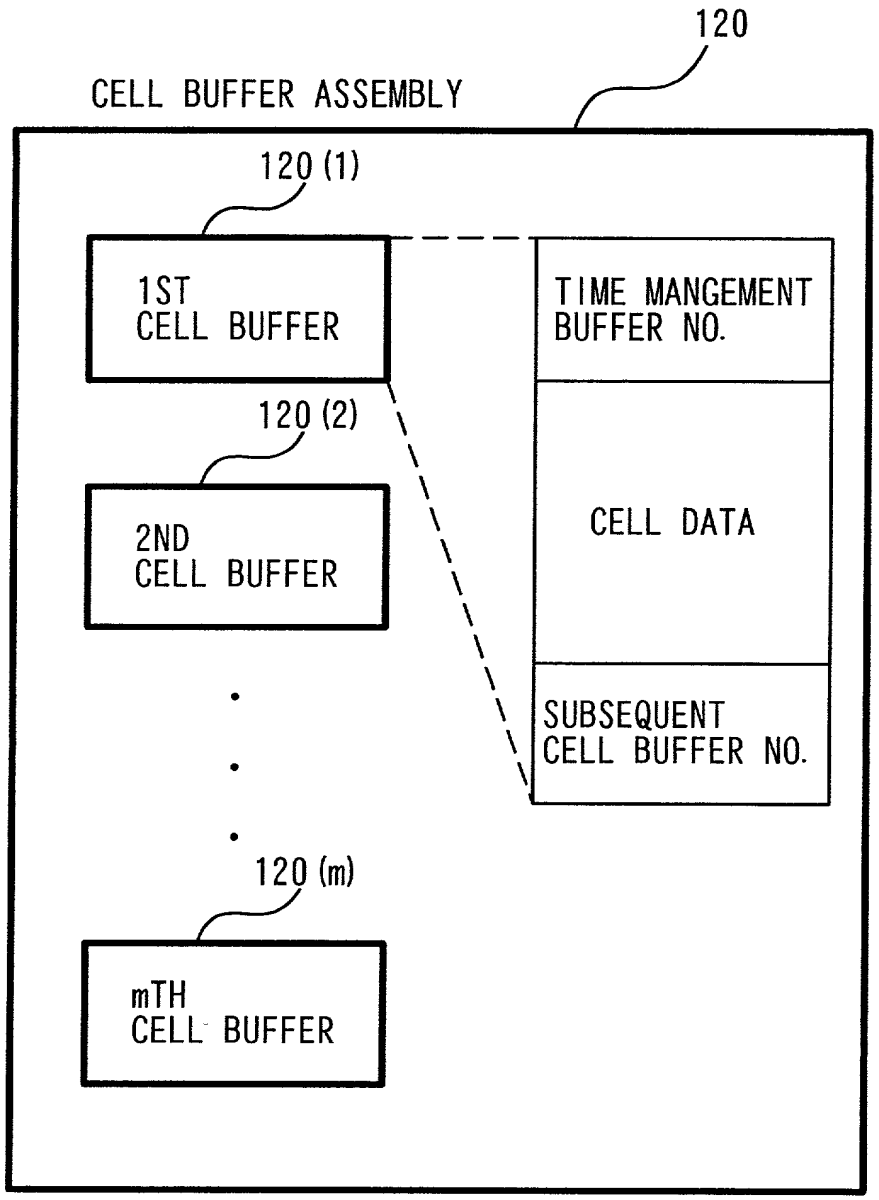

120
CELL BUFFER ASSEMBLY
120 (1)
1ST
CELL BUFFER
120 (2)
2ND
CELL BUFFER
120 (m)
mTH
CELL BUFFER
TIME MANGEMENT
BUFFER NO.
CELL DATA
SUBSEQUENT
CELL BUFFER NO.

Fig. 5

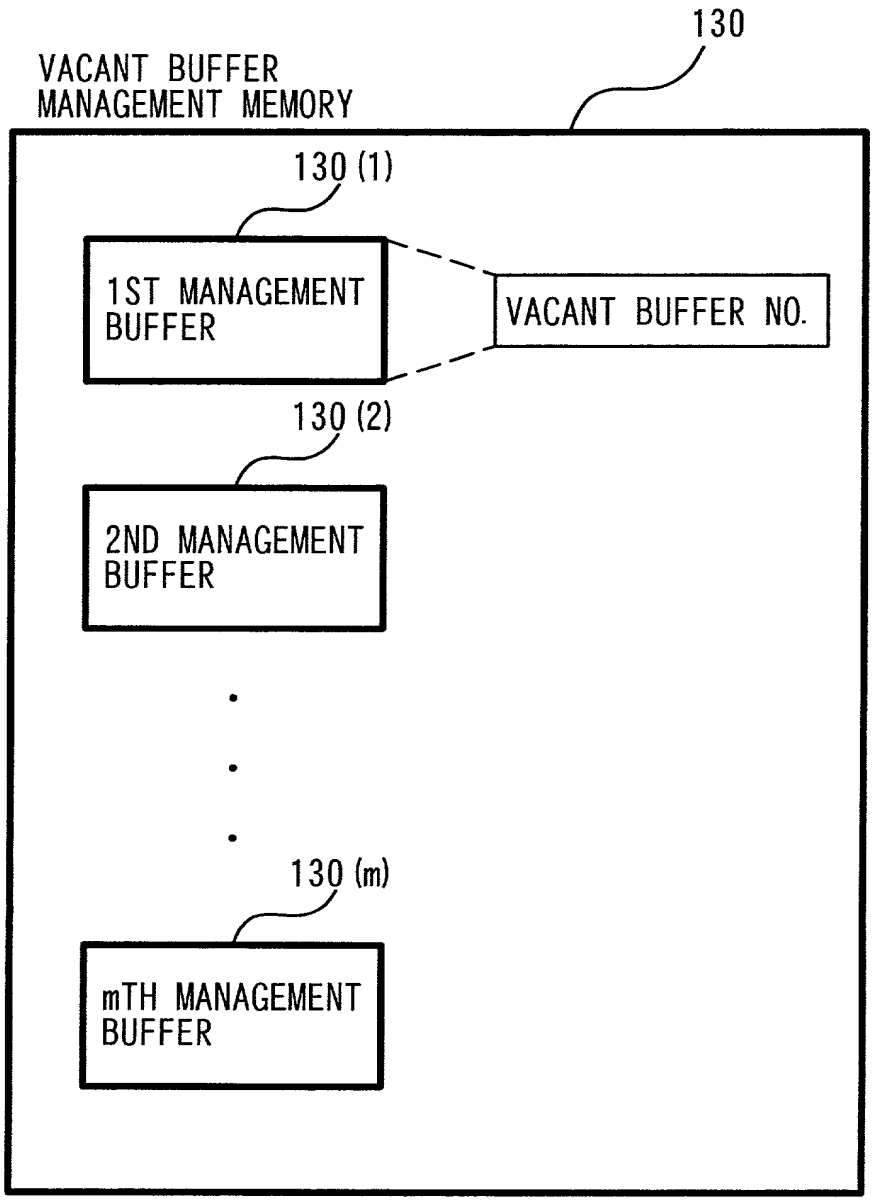

130
VACANT BUFFER
MANAGEMENT MEMORY
130 (1)
1ST MANAGEMENT
BUFFER
VACANT BUFFER NO.
130 (2)
2ND MANAGEMENT
BUFFER
130 (m)
mTH MANAGEMENT
BUFFER

Fig. 6

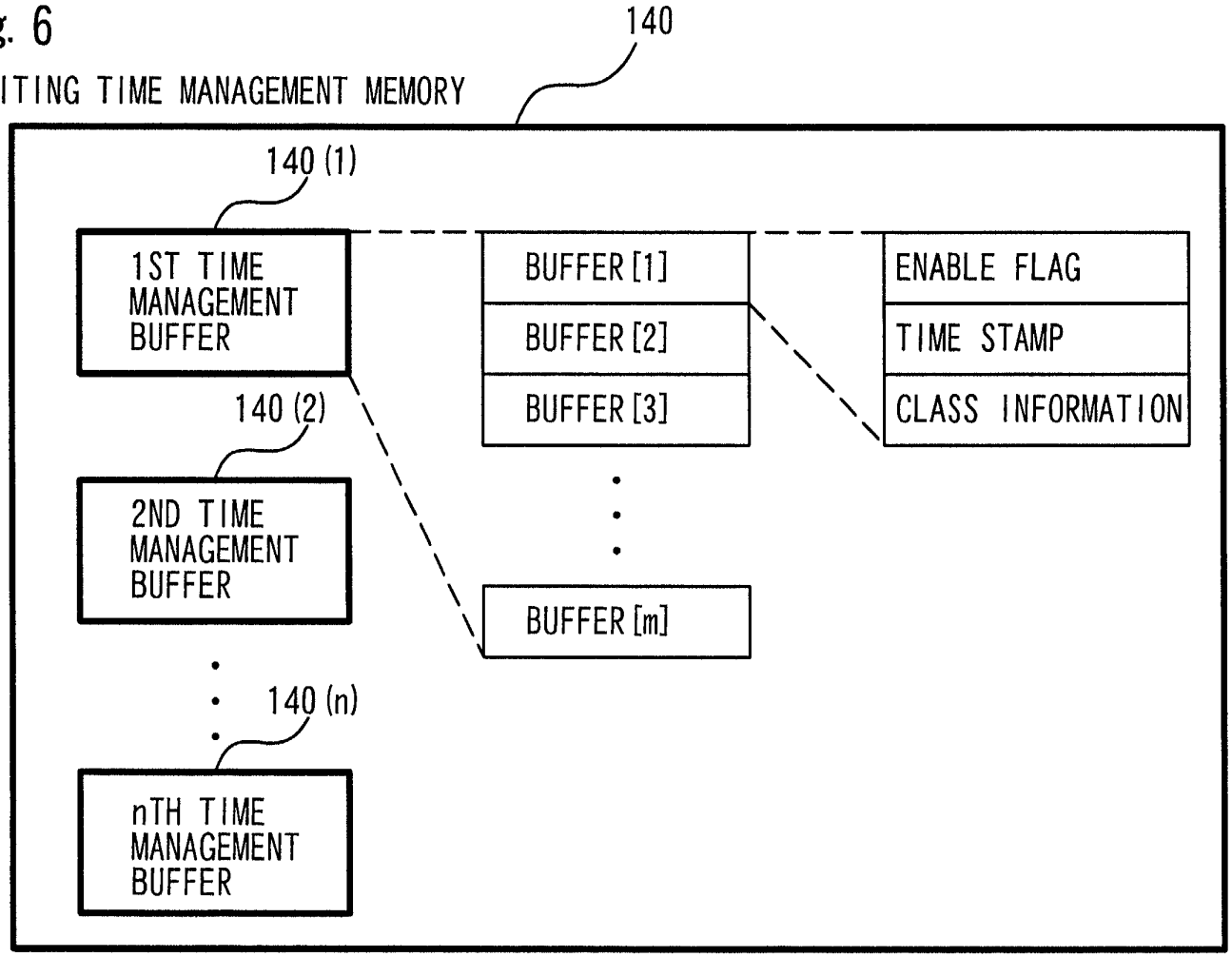

140
WRITING TIME MANAGEMENT MEMORY
140 (1)
1ST TIME MANAGEMENT BUFFER
140 (2)
2ND TIME MANAGEMENT BUFFER
140 (n)
nTH TIME MANAGEMENT BUFFER
BUFFER [1]
BUFFER [2]
BUFFER [3]
BUFFER [m]
ENABLE FLAG
TIME STAMP
CLASS INFORMATION

Fig. 7

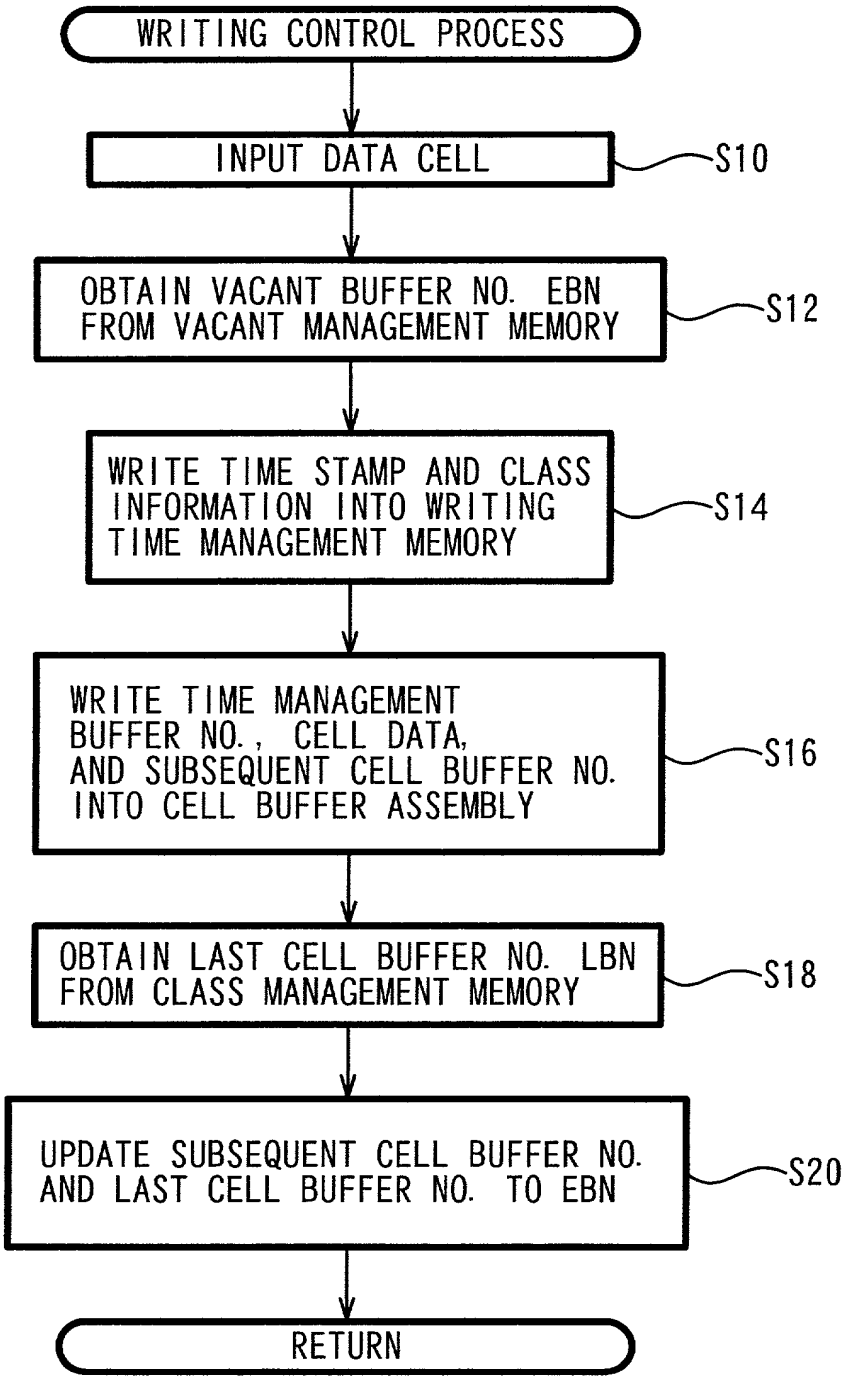

WRITING CONTROL PROCESS
INPUT DATA CELL
S10
OBTAIN VACANT BUFFER NO. EBN FROM VACANT MANAGEMENT MEMORY
S12
WRITE TIME STAMP AND CLASS INFORMATION INTO WRITING TIME MANAGEMENT MEMORY
S14
WRITE TIME MANAGEMENT BUFFER NO., CELL DATA, AND SUBSEQUENT CELL BUFFER NO. INTO CELL BUFFER ASSEMBLY
S16
OBTAIN LAST CELL BUFFER NO. LBN FROM CLASS MANAGEMENT MEMORY
S18
UPDATE SUBSEQUENT CELL BUFFER NO. AND LAST CELL BUFFER NO. TO EBN
S20
RETURN

Fig. 8

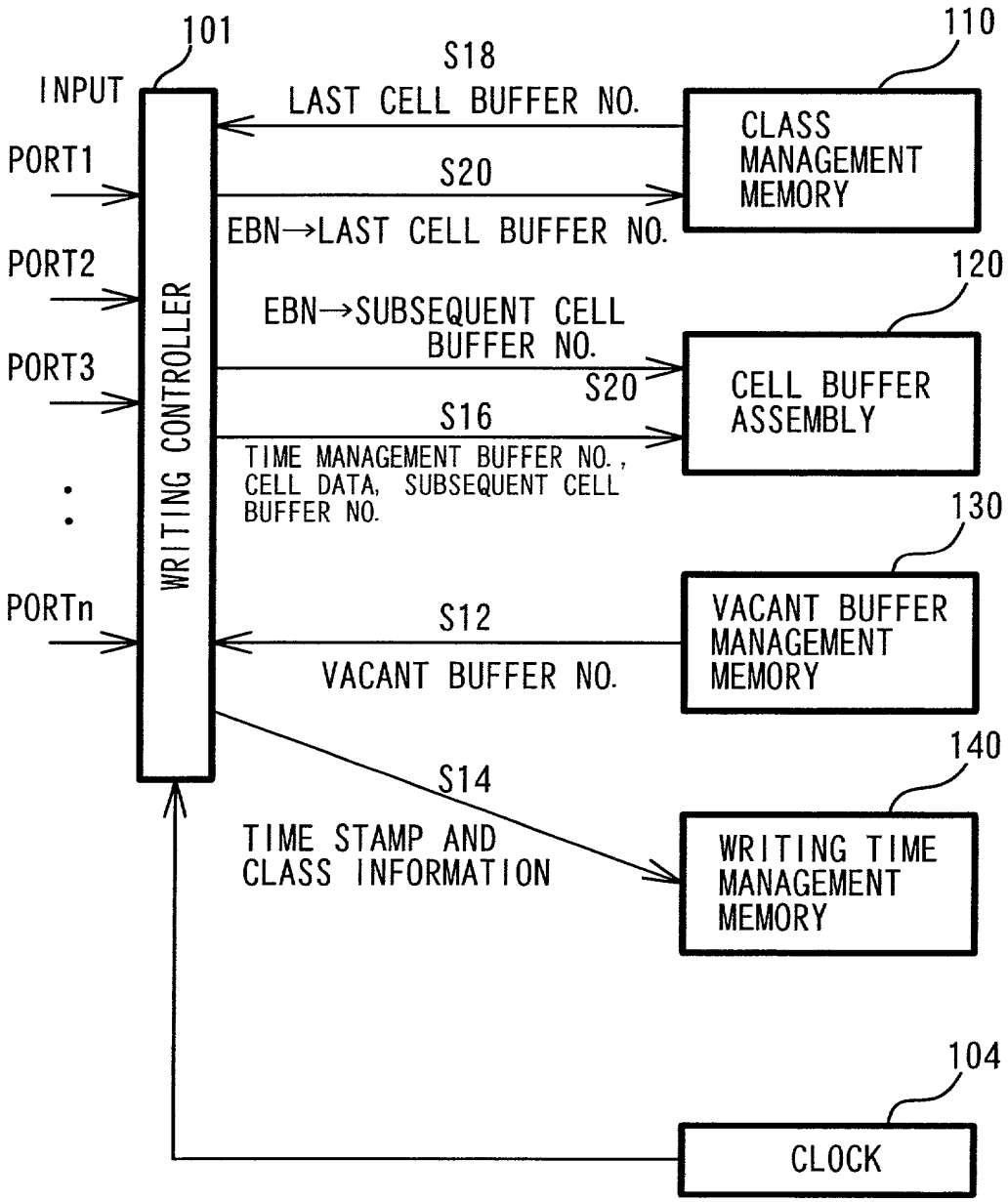

101
110
S18
INPUT
LAST CELL BUFFER NO.
CLASS MANAGEMENT MEMORY
PORT1
S20
EBN→LAST CELL BUFFER NO.
PORT2
120
EBN→SUBSEQUENT CELL BUFFER NO.
PORT3
S20
CELL BUFFER ASSEMBLY
S16
TIME MANAGEMENT BUFFER NO., CELL DATA, SUBSEQUENT CELL BUFFER NO.
WRITING CONTROLLER
130
PORTn
S12
VACANT BUFFER MANAGEMENT MEMORY
VACANT BUFFER NO.
140
S14
TIME STAMP AND CLASS INFORMATION
WRITING TIME MANAGEMENT MEMORY
104
CLOCK

Fig.9

			Initial	S14	S16	S20
1ST Class Management Buffer	Head cell buffer No.		1	1	1	1
	Last cell buffer No.		1	1	1	3
1ST Cell Buffer	Time management buffer No.		1	1	1	1
	Cell data		AAA	AAA	AAA	AAA
	Subsequent cell buffer No.		1	1	1	3
2ND Cell Buffer	Time management buffer No.					
	Cell data					
	Subsequent cell buffer No.					
3rd Cell Buffer	Time management buffer No.				2	2
	Cell data				BBB	BBB
	Subsequent cell buffer No.				3	3
4th Cell Buffer	Time management buffer No.					
	Cell data					
	Subsequent cell buffer No.					
Vacant Buffer Management Memory	1ST management buffer		3			
	2ND management buffer		4	4	4	4
	3rd management buffer		2	2	2	2
	4th management buffer					
1ST Time Management Buffer	Buffer[1]	Enable flag	1	1	1	1
		Time stamp	aa:aa	aa:aa	aa:aa	aa:aa
		Class information	1	1	1	1
	Buffer[2]	Enable flag	0	1	1	1
		Time stamp		bb:bb	bb:bb	bb:bb
		Class information		1	1	1
	Buffer[3]	Enable flag	0	0	0	0
		Time stamp				
		Class information				
	Buffer[4]	Enable flag	0	0	0	0
		Time stamp				
		Class information				

Fig. 10

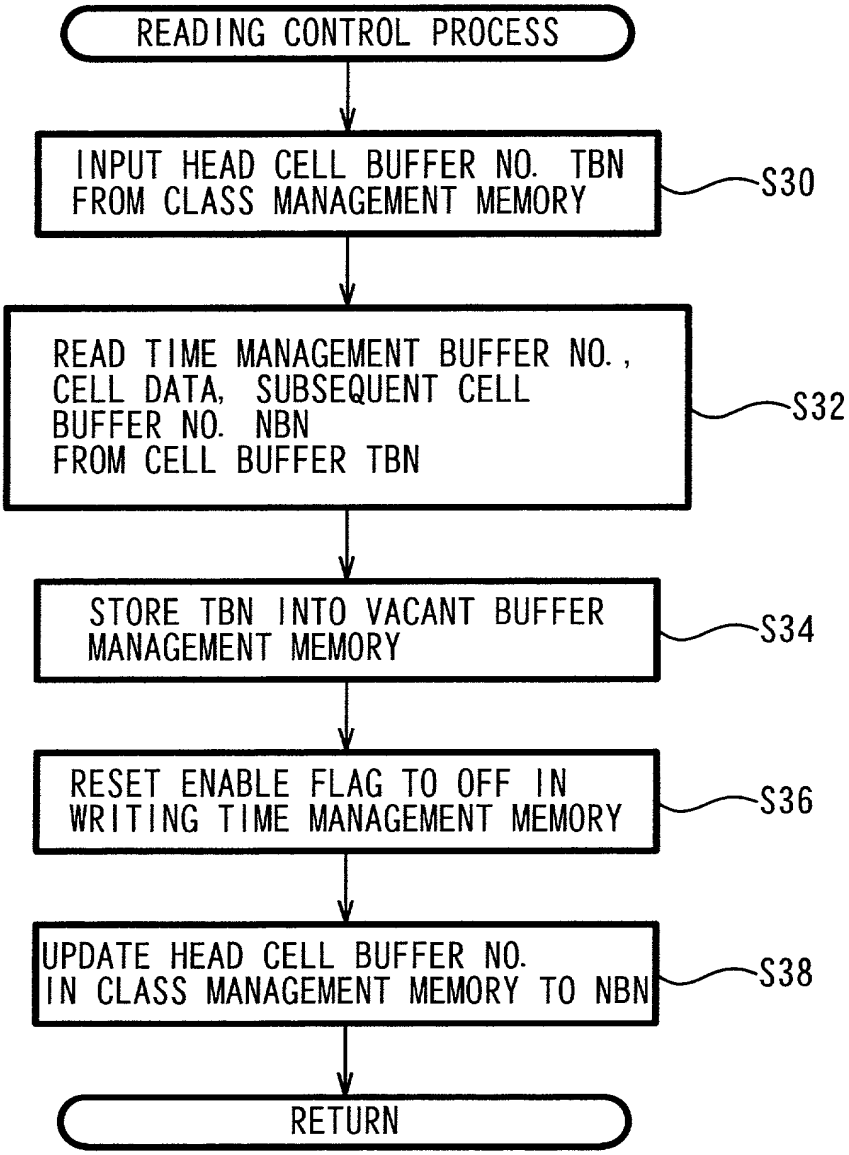

READING CONTROL PROCESS
INPUT HEAD CELL BUFFER NO. TBN FROM CLASS MANAGEMENT MEMORY
S30
READ TIME MANAGEMENT BUFFER NO., CELL DATA, SUBSEQUENT CELL BUFFER NO. NBN FROM CELL BUFFER TBN
S32
STORE TBN INTO VACANT BUFFER MANAGEMENT MEMORY
S34
RESET ENABLE FLAG TO OFF IN WRITING TIME MANAGEMENT MEMORY
S36
UPDATE HEAD CELL BUFFER NO. IN CLASS MANAGEMENT MEMORY TO NBN
S38
RETURN

Fig. 11

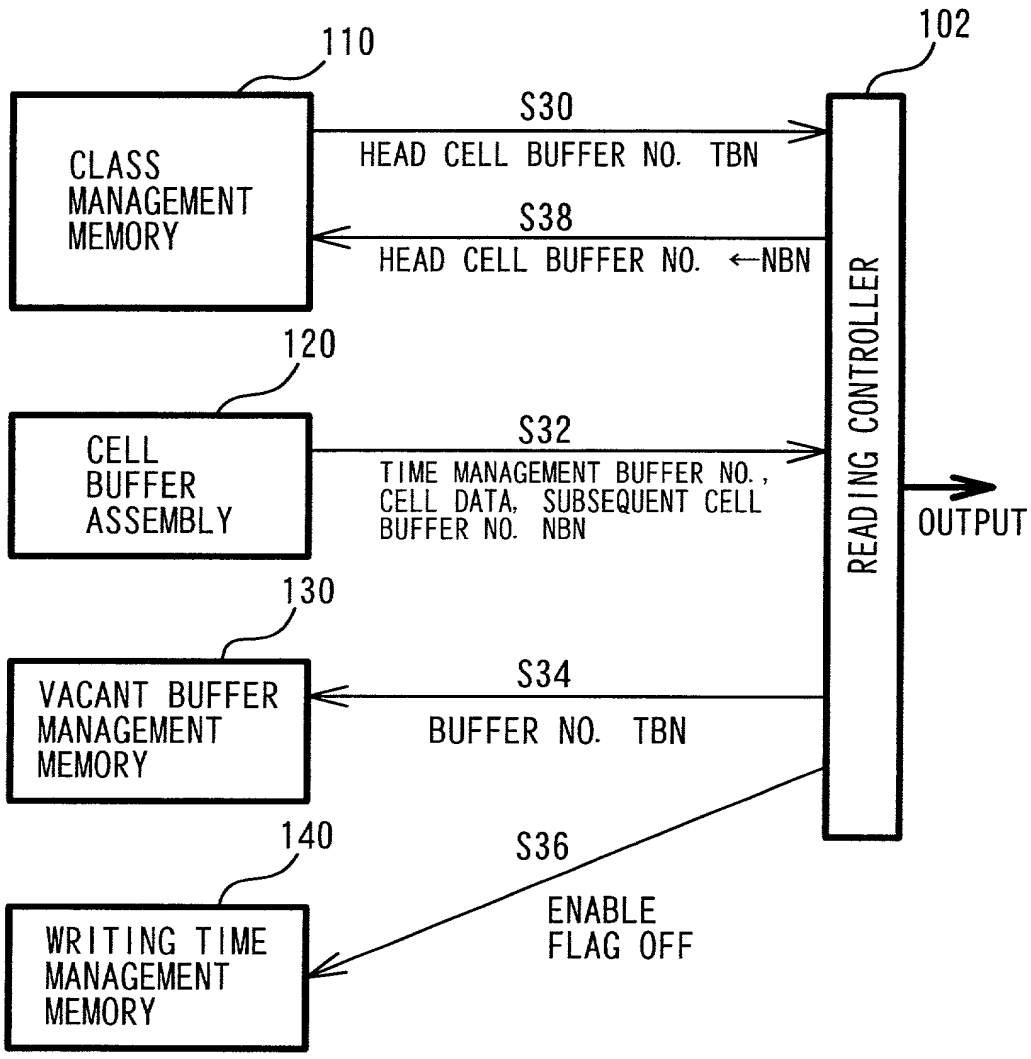

110
CLASS MANAGEMENT MEMORY
S30
HEAD CELL BUFFER NO. TBN
S38
HEAD CELL BUFFER NO. ←NBN
102
READING CONTROLLER
OUTPUT
120
CELL BUFFER ASSEMBLY
S32
TIME MANAGEMENT BUFFER NO., CELL DATA, SUBSEQUENT CELL BUFFER NO. NBN
130
VACANT BUFFER MANAGEMENT MEMORY
S34
BUFFER NO. TBN
140
WRITING TIME MANAGEMENT MEMORY
S36
ENABLE FLAG OFF

Fig.12

			Initial	S32	S34	S36	S38
1ST Class Management Buffer	Head cell buffer No.		1	1	1	1	3
	Last cell buffer No.		3	3	3	3	3
1ST Cell Buffer	Time management buffer No.		1				
	Cell data		AAA				
	Subsequent cell buffer No.		3				
2ND Cell Buffer	Time management buffer No.						
	Cell data						
	Subsequent cell buffer No.						
3rd Cell Buffer	Time management buffer No.		2	2	2	2	2
	Cell data		BBB	BBB	BBB	BBB	BBB
	Subsequent cell buffer No.		3	3	3	3	3
4th Cell Buffer	Time management buffer No.						
	Cell data						
	Subsequent cell buffer No.						
Vacant Buffer Management Memory	1ST management buffer						
	2ND management buffer		4	4	4	4	4
	3rd management buffer		2	2	2	2	2
	4th management buffer				1	1	1
1ST Time Management Buffer	Buffer[1]	Enable flag	1	1	1	0	0
		Time stamp	aa:aa	aa:aa	aa:aa		
		Class information	1	1	1		
	Buffer[2]	Enable flag	1	1	1	1	1
		Time stamp	bb:bb	bb:bb	bb:bb	bb:bb	bb:bb
		Class information	1	1	1	1	1
	Buffer[3]	Enable flag	0	0	0	0	0
		Time stamp					
		Class information					
	Buffer[4]	Enable flag	0	0	0	0	0
		Time stamp					
		Class information					

Fig. 13

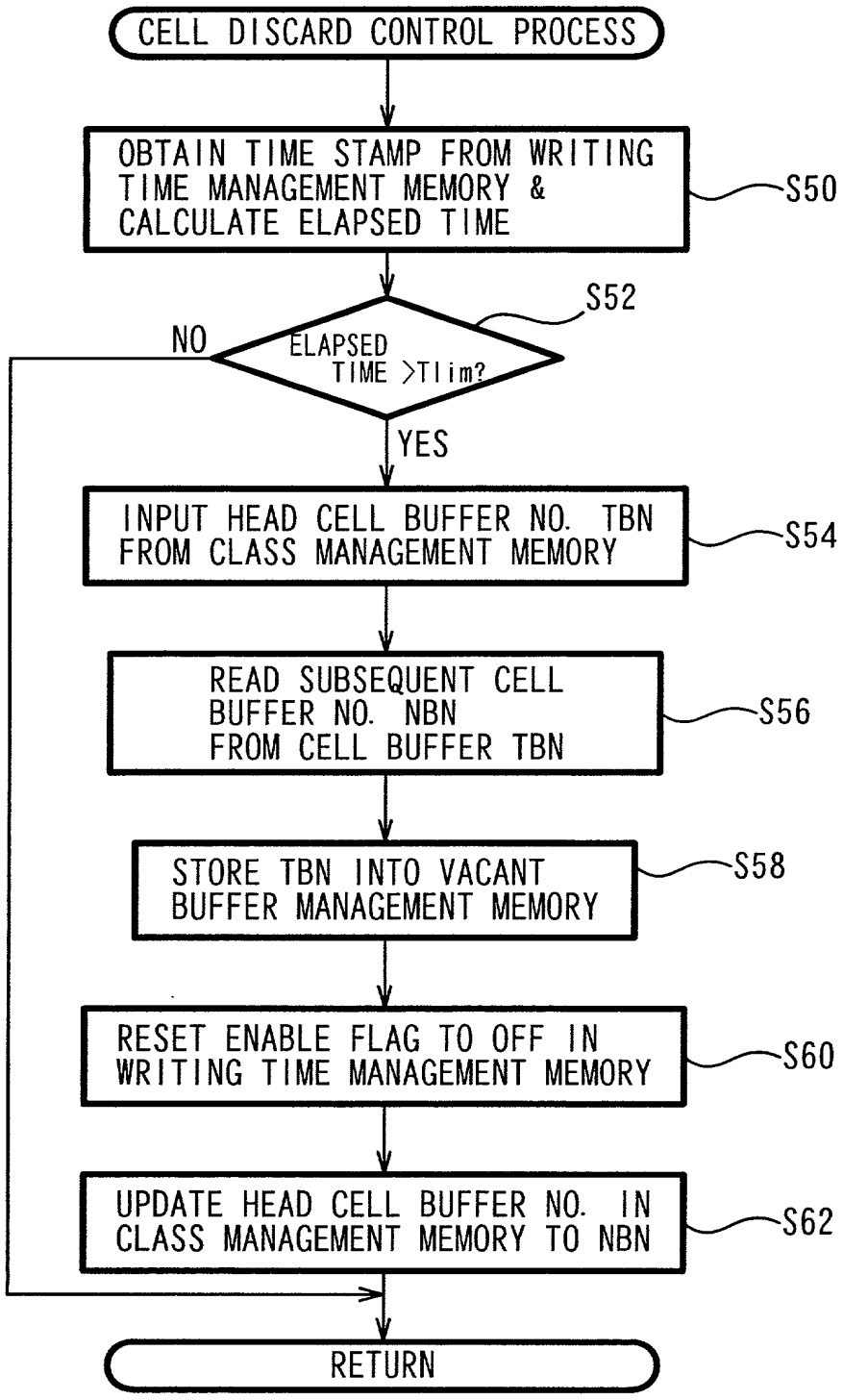

CELL DISCARD CONTROL PROCESS
OBTAIN TIME STAMP FROM WRITING TIME MANAGEMENT MEMORY & CALCULATE ELAPSED TIME
S50
S52
NO
ELAPSED TIME >Tlim?
YES
INPUT HEAD CELL BUFFER NO. TBN FROM CLASS MANAGEMENT MEMORY
S54
READ SUBSEQUENT CELL BUFFER NO. NBN FROM CELL BUFFER TBN
S56
STORE TBN INTO VACANT BUFFER MANAGEMENT MEMORY
S58
RESET ENABLE FLAG TO OFF IN WRITING TIME MANAGEMENT MEMORY
S60
UPDATE HEAD CELL BUFFER NO. IN CLASS MANAGEMENT MEMORY TO NBN
S62
RETURN

Fig. 14

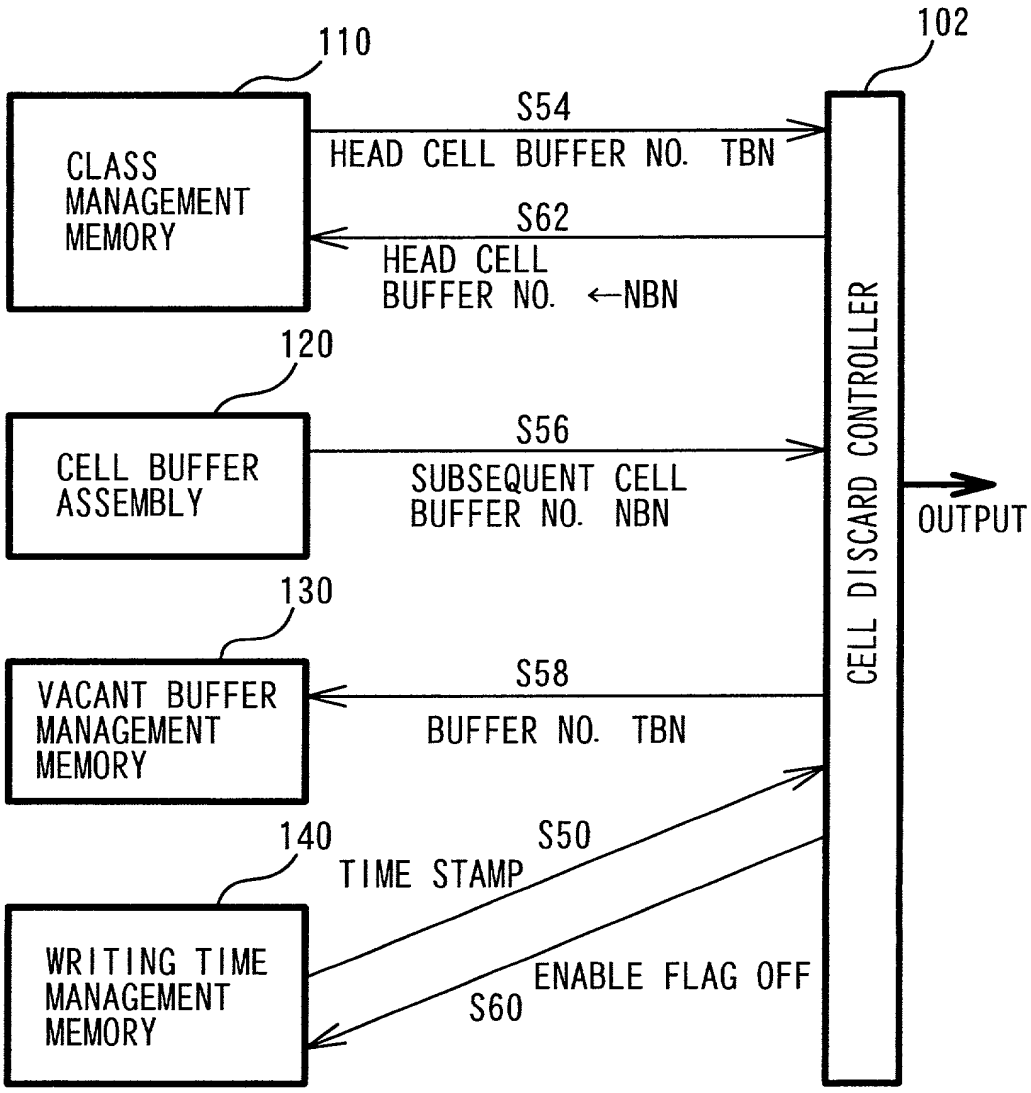

110
102
CLASS MANAGEMENT MEMORY
S54
HEAD CELL BUFFER NO. TBN
S62
HEAD CELL BUFFER NO. ←NBN
120
CELL BUFFER ASSEMBLY
S56
SUBSEQUENT CELL BUFFER NO. NBN
CELL DISCARD CONTROLLER
OUTPUT
130
VACANT BUFFER MANAGEMENT MEMORY
S58
BUFFER NO. TBN
140
S50
TIME STAMP
WRITING TIME MANAGEMENT MEMORY
ENABLE FLAG OFF
S60

Fig.15

			Initial	S56	S58	S60	S62
1ST Class Management Buffer	Head cell buffer No.		1	1	1	1	3
	Last cell buffer No.		3	3	3	3	3
1ST Cell Buffer	Time management buffer No.		1	1	1	1	
	Cell data		AAA	AAA	AAA	AAA	
	Subsequent cell buffer No.		3	3	3	3	
2ND Cell Buffer	Time management buffer No.						
	Cell data						
	Subsequent cell buffer No.						
3rd Cell Buffer	Time management buffer No.		2	2	2	2	2
	Cell data		BBB	BBB	BBB	BBB	BBB
	Subsequent cell buffer No.		3	3	3	3	3
4th Cell Buffer	Time management buffer No.						
	Cell data						
	Subsequent cell buffer No.						
Vacant Buffer Management Memory	1ST management buffer						
	2ND management buffer		4	4	4	4	4
	3rd management buffer		2	2	2	2	2
	4th management buffer				1	1	1
1ST Time Management Buffer	Buffer[1]	Enable flag	1	1	1	0	0
		Time stamp	aa:aa	aa:aa	aa:aa		
		Class information	1	1	1		
	Buffer[2]	Enable flag	1	1	1	1	1
		Time stamp	bb:bb	bb:bb	bb:bb	bb:bb	bb:bb
		Class information	1	1	1	1	1
	Buffer[3]	Enable flag	0	0	0	0	0
		Time stamp					
		Class information					
	Buffer[4]	Enable flag	0	0	0	0	0
		Time stamp					
		Class information					

Fig. 16

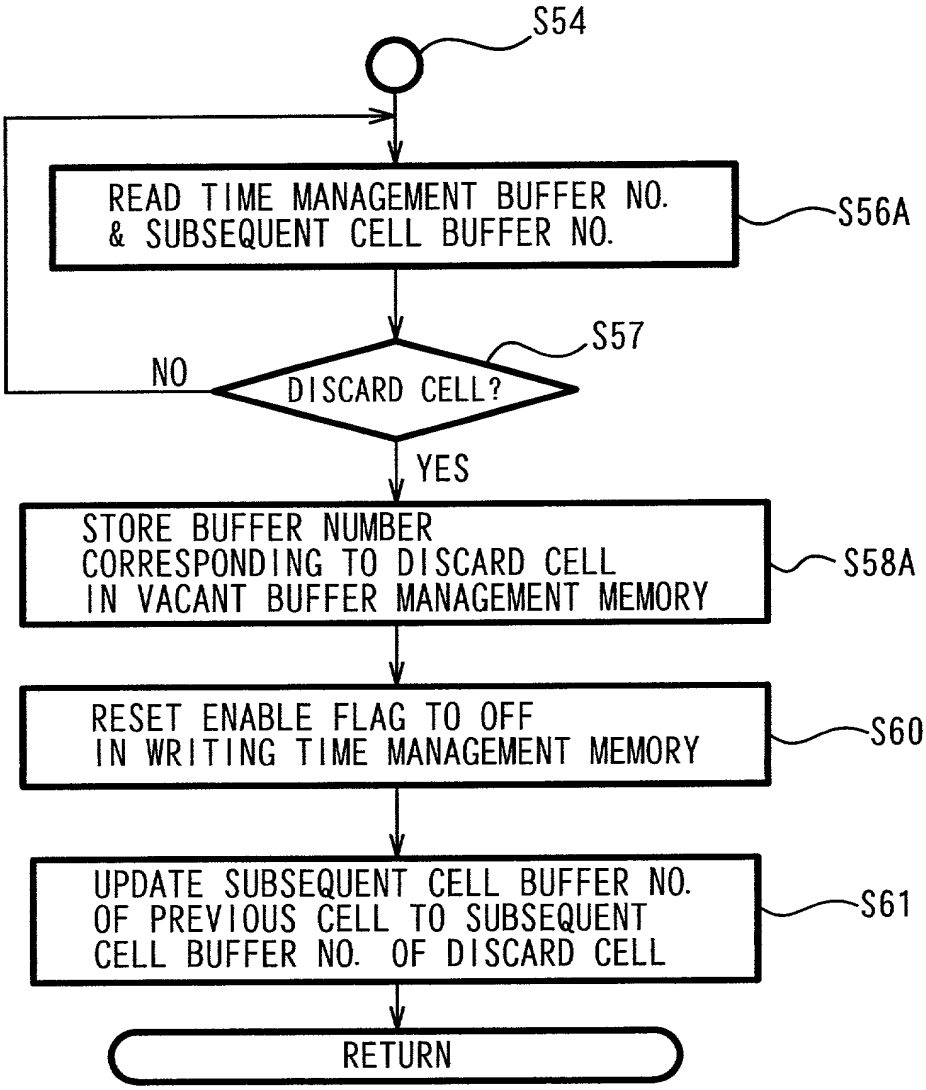

S54
READ TIME MANAGEMENT BUFFER NO.
& SUBSEQUENT CELL BUFFER NO.
S56A
S57
NO
DISCARD CELL?
YES
STORE BUFFER NUMBER
CORRESPONDING TO DISCARD CELL
IN VACANT BUFFER MANAGEMENT MEMORY
S58A
RESET ENABLE FLAG TO OFF
IN WRITING TIME MANAGEMENT MEMORY
S60
UPDATE SUBSEQUENT CELL BUFFER NO.
OF PREVIOUS CELL TO SUBSEQUENT
CELL BUFFER NO. OF DISCARD CELL
S61
RETURN

Fig. 17

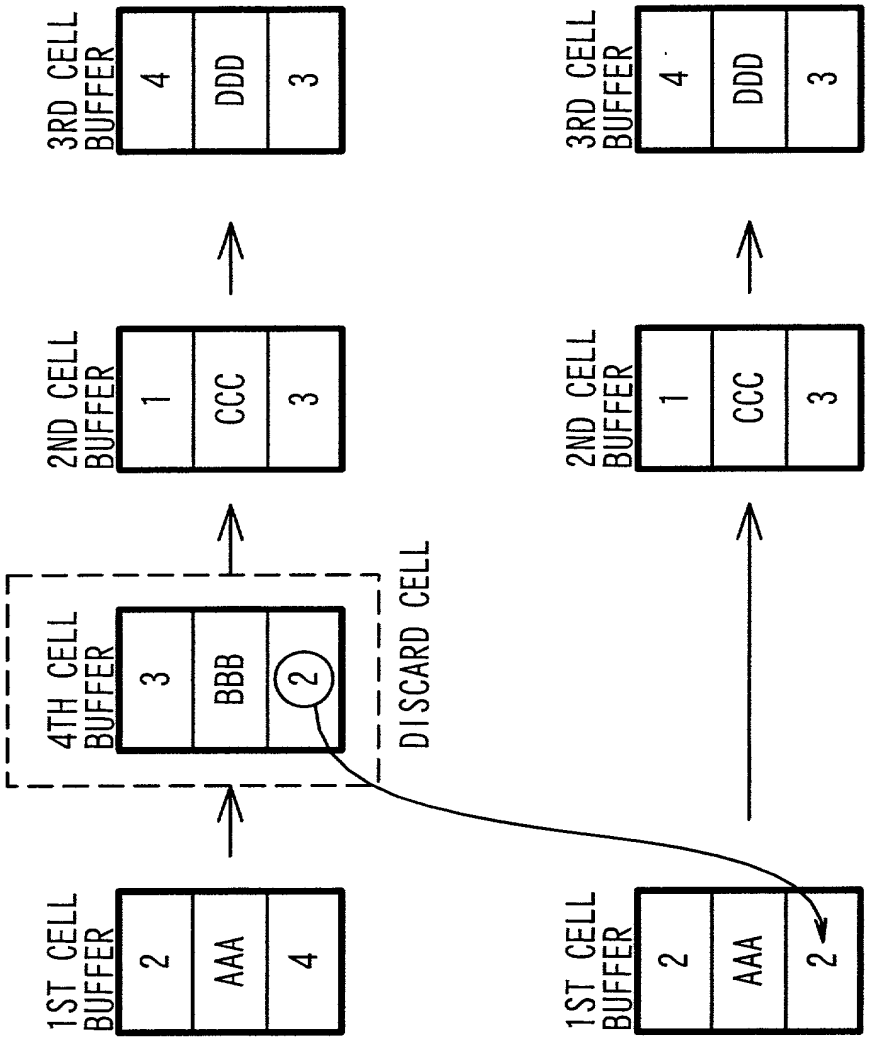
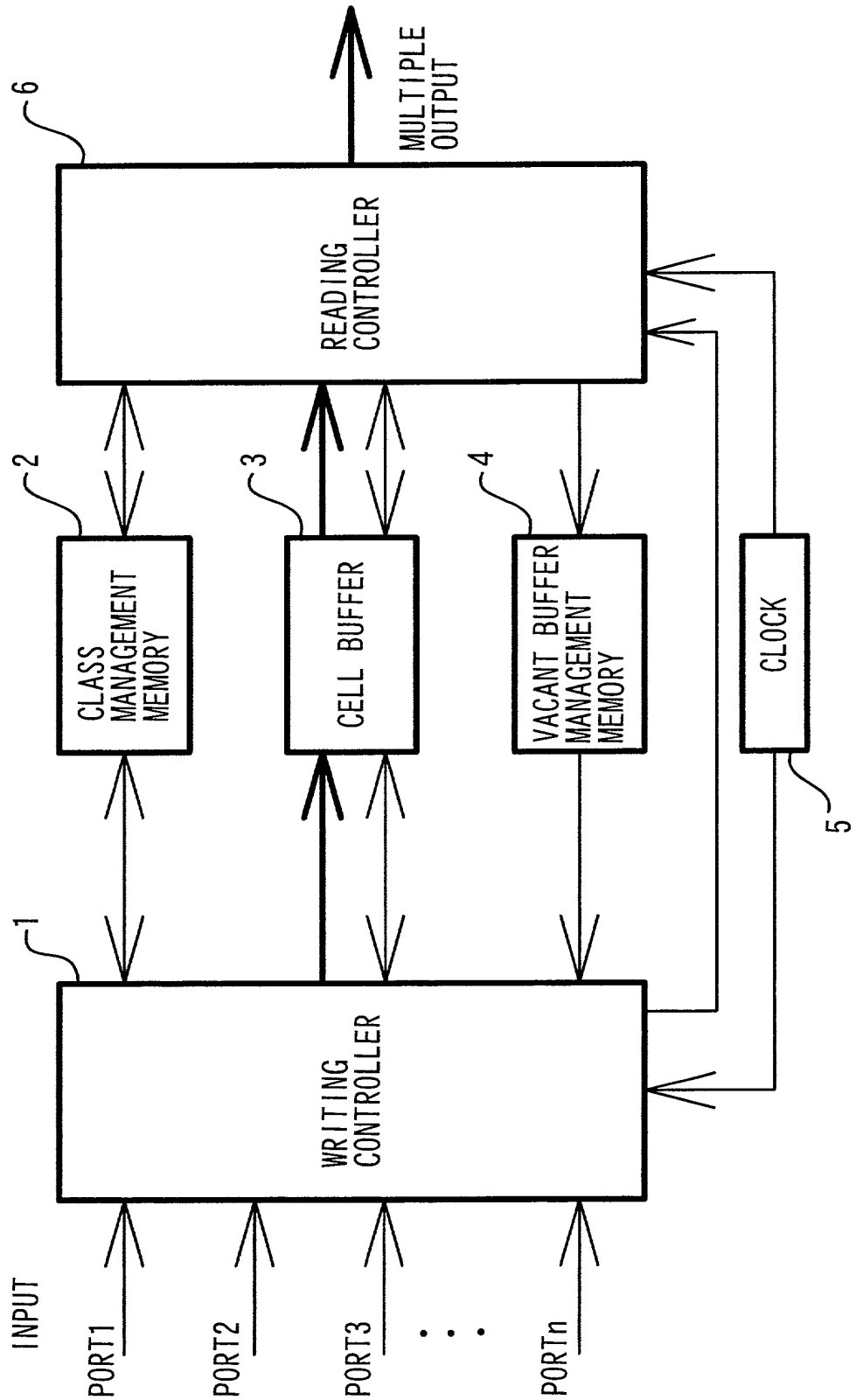

1ST CELL BUFFER
2
AAA
4
4TH CELL BUFFER
3
BBB
2
DISCARD CELL
2ND CELL BUFFER
1
CCC
3
3RD CELL BUFFER
4
DDD
3
1ST CELL BUFFER
2
AAA
2
2ND CELL BUFFER
1
CCC
3
3RD CELL BUFFER
4
DDD
3

Fig. 18


INPUT
PORT1
PORT2
PORT3
PORTn
WRITING CONTROLLER
1
CLASS MANAGEMENT MEMORY
2
CELL BUFFER
3
VACANT BUFFER MANAGEMENT MEMORY
4
CLOCK
5
READING CONTROLLER
6
MULTIPLE OUTPUT